IN THE CLAIMS

Please amend the claims as follows:

1. (original) A signal comprising a runlength limited (RLL) encoded binary *d,k* channel bitstream (3), wherein parameter *d* defines a minimum number and parameter *k* defines a maximum number of zeroes between any two ones of said bitstream (3) or vice versa, comprising

a number of sections of respectively *N* successive RLL channel bits, called RLL rows (8-13, 45), each RLL row (8-13, 45) representing a parity-check code-word, called row parity-check code-word, in which a so-called row-based parity-check constraint for said RLL row (8-13, 45) has been realized;

characterized in that

K sections of respectively *N* successive channel bits, called column parity-check rows (21, 22, 43, 44, 46), are located at predetermined positions of a group of *M* RLL rows (8-13, 45), *K*, *N* and *M* being integer values, said column parity-check rows (21, 22, 43, 44, 46) comprising a plurality of column parity-check enabling channel words (30, 42, 48),

wherein each of said column parity-check enabling channel words (30, 42, 48) realizes a so-called column-based parity-check constraint for all so-called corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) of said group that correspond to a specific column parity-check enabling channel word (30, 42, 48), hereby constituting a column parity-check codeword.

2. (original) A signal according to claim 1, characterized in that the number *K* of column parity-check rows (21, 22, 43, 44, 46) is at least 2.

3. (original) A signal according to claim 1, characterized in that each one of said row parity-check code-words comprises a row parity-check enabling channel word (15-20) being appended to RLL encoded user data without itself containing user data.

4. (original) A signal according to claim 1, characterized in that each one of said row parity-check code-words comprises a row parity-check enabling channel word (15-20) being encoded user data.

5. (original) A signal according to claim 1, characterized in that each of said row parity-check code-words comprises a parity-check bit p_{2H} realizing the row-based parity-check constraint

$$p_{2H} = Mod\left[\sum_{i=0}^{N-1} i \cdot b_i, 2\right]$$

which is at an encoder set to a predetermined value, known at an decoder, that is, it is either set to 0 or to 1, with b_i being successive bits of said d,k channel bitstream (3) of an RLL row (8-13, 45).

6. (original) A signal according to claim 1, characterized in that said corresponding segments (24-29) of RLL rows (8-13, 45) being respectively a certain bit at a predetermined position of each of said RLL rows (8-13, 45) and a respective single-bit wide column parity-check enabling channel word or words (30, 42, 48) is or are located at the same position of each of said K column parity-check rows (21, 22, 43, 44, 46).

7. (original) A signal according to claim 6, characterized in that the number K of column parity-check rows (21, 22, 43, 44, 46) is an integer value with $K \geq 1/R$, with R being the code rate of the RLL code with RLL constraints d and k.

8. (original) A signal according to claim 7, characterized in that each of said single-bit wide column parity-check enabling channel words (30, 42, 48) is an encoded symbol of a parity-check bit p_{2v} realizing the column-based parity-check constraint

$$p_{2v} = \mathrm{mod}\left[\sum_{l=0}^{M+K-1} b_l, 2\right]$$

which is at the encoder set to a predetermined value, known at the decoder, that is, either set to 0 or to 1, with b_l being bits of the RLL rows (8-13, 45) of said group at a certain position, wherein the bits of said symbol are spread over said K column parity-check rows (21, 22, 43, 44, 46), one bit per row.

9. (original) A signal according to claim 8, characterized in that said symbol is selected from a number of different symbols realizing said column-based parity-check constraint p_{2v} in order to realize the d,k constraints of the RLL code within said column parity-check rows (21, 22, 43, 44, 46) as well.

10. (original) A signal according to claim 6, characterized in that said single-bit wide column parity-check enabling channel words (30, 42, 48) are located at each channel bit position of a column parity-check row (21, 22, 43, 44, 46), hereby constituting at every bit-wide column a column parity-check codeword.

11. (original) A signal according to claim 6, characterized in that said single-bit wide column parity-check enabling channel words (30, 42, 48) are located at every second channel bit position only, hereby constituting at every second bit-wide column a column parity-check codeword.

12. (original) A signal according to claim 11, characterized in that channel bits between said second bit positions are used as

merging bits in order to realize said *d,k* constraints of said RLL code and/or any desired spectral property of the code like DC-control.

13. (original) A signal according to claim 1, characterized in that said predetermined position of a row parity-check enabling channel word (15-20) is at the end of an RLL row (8-13, 45).

14. (original) A signal according to claim 1, characterized in that said *K* column parity-check rows (21, 22, 43, 44, 46) are arranged successively.

15. (original) A signal according to claim 1, characterized in that said *M* RLL rows (8-13, 45) are arranged successively.

16. (original) A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows (21, 22, 43, 44, 46) is at the end of said group.

17. (original) A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows (21, 22, 43, 44, 46) is in front of said group.

18. (original) A signal according to claim 1, characterized in that said predetermined position of said *K* column parity-check rows (21, 22, 43, 44, 46) is within said group.

19. (original) A signal according to claim 1, characterized in that the number *K* of column parity-check rows (43, 44, 46) is two,

each of said column parity-check rows is divided into segments (48-50) of at least two types, and in the case of two types, of more than one successive channel bits of alternating segment width

N_1 or N_2, N_1 and N_2 being integer values, N_1 being the width of the first column parity-check segment and N_2 being the width of the second parity-check segment,

wherein in each column parity-check row (43, 44, 46) only every second segment (48-50) is a column parity-check enabling channel word (48) and

wherein only one of both column parity-check rows (43, 44, 46) starts with a column parity-check enabling channel word (48),

whereas in the other column parity-check row the first column parity-check enabling channel word (48) is at the second segment position.

20. (original) A signal according to claim 19, characterized in that within each column parity-check row (21, 22, 43, 44, 46) the so-called merging segments (49, 50) in front of or behind a column parity-check enabling channel word (48) do not contain any user data, but are designed such to realize said d,k constraints of said RLL code and/or any desired spectral property of the code like DC-control.

21. (original) A signal according to claim 19, characterized in that in the first one of both column parity-check rows (43) the parity-check information of each column parity-check enabling channel word (48) realizes said parity-check constraint only for said column parity-check enabling channel word (48) in addition to said corresponding segments of said M RLL rows (8-13, 45) of said group.

22. (original) A signal according to claim 21, characterized in that in the second one of both column parity-check rows (44) the parity-check information of each column parity-check enabling channel word (48) realizes said parity-check constraint only for

said column parity-check enabling channel word (48) in addition to said corresponding segments of said *M* RLL rows (8-13, 45) of said group.

23. (original) A signal according to claim 21, characterized in that in the second one of both column parity-check rows (44) the parity-check information of each column parity-check enabling channel word (48) realizes said parity-check constraint for said column parity-check enabling channel word (48) as well as the corresponding merging segment (49) of said first column parity-check row (43) in addition to said corresponding segment of said *M* RLL rows (8-13, 45) of said group.

24. (original) A signal according to claim 19, characterized in that said segment or channel word widths N_1 and N_2 are in the range of $d \leq N_{1,2} \leq k$.

25. (currently amended) A signal according to claim 21 ~~or 22~~, characterized in that said parity-check constraint is

$$V = \mathrm{Mod}\left[\sum_{j=1}^{M+1} w_j, q_1\right]$$

being set to a predetermined value at the encoder, known at the decoder, and is preferably set to 0, wherein j is a unique index associated with each RLL row (8-13, 45) for $1 \leq j \leq M$ and an index associated with the actual column parity-check row for $j = M + 1$, and

wherein w_j is a unique index associated with each word W_j which defines one of a number of possible d,k constrained sequences of said segment width (N_1, N_2), wherein such a word W_j is comprised in each corresponding segment.

26. (original) A signal according to claim 23, characterized in that said column based parity-check constraint is

$$V = \mathrm{Mod}\left[\sum_{j=1}^{M+2} w_j, q_1\right]$$

being set to a predetermined value at the encoder, known at the decoder, and is preferably set to 0, wherein j is a unique index associated with each RLL row for $1 \leq j \leq M$ and with each column parity-check row for $j = M + 1$, $M + 2$, and wherein w_j is a unique index associated with each word W_j which defines one of the a number of possible d,k constrained sequences of said segment width (N_1, N_2), wherein such a word W_j is comprised in each corresponding segment.

27. (currently amended) A signal according to claim 25 ~~or 26~~, characterized in that said unique index w_j is

$$w_j = \sum_{i=0}^{N_{1,2}-1} b_i^j \cdot N_d(i)$$

wherein b_i^j denotes bit number i of word W_j in row j and wherein $N_d(i)$ is the number of possible d,k constrained sequences of length i.

28. (original) A signal according to claim 1, characterized by a waveform comprising said d,k channel bitstream, wherein said waveform transitions between two states (land, pit) whenever a one occurs in said d,k channel bitstream (3) and keeps its actual state whenever a zero occurs in said d,k channel bitstream (3) or vice versa.

29. (original) A storage medium storing a signal according to any one of claims 1 to 28.

30. (original) A storage medium according to claim 29, characterized in that said storage medium is a recorded optical, magnetic, or magneto-optical disc or recoded magnetic tape.

31. (currently amended) A method for encoding a stream of user data bits comprising the steps of:

runlength limited (RLL) encoding said stream of user data bits into a binary *d,k* channel bitstream (3) comprising a number of sections of respectively *N* successive RLL channel bits, called RLL rows (8-13, 45), wherein parameter *d* defines a minimum number and parameter *k* defines a maximum number of zeroes between any two ones of said bitstream (3) or vice versa,

each RLL row (8-13, 45) ~~respesenting~~ representing a parity-check code-word, called row parity-check code-word in which a so-called row-based parity-check constraint for said RLL row (8-13, 45) has been realized,

characterized by the further step of

generating *K* sections of respectively *N* successive channel bits, called column parity-check rows (21, 22, 43, 44, 46), at predetermined positions of a group of *M* RLL rows (8-13, 45), *K*, *N* and *M* being integer values, said column parity-check rows (21, 22, 43, 44, 46) comprising a plurality of column parity-check enabling channel words (30, 42, 48),

wherein each of said column parity-check enabling channel words (30, 42, 48) realizes a so-called column-based parity-check constraint for so-called corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) of said group that correspond to a specific column parity-check enabling channel word (30, 42, 48), hereby constituting a column parity-check codeword.

32. (currently amended) A method according to claim 31, characterized by generating a signal according to any one of claims 1 to ~~30~~ 28 or 49 to 51.

33. (original) A device for encoding a stream of user data bits comprising:

encoding means for runlength limited (RLL) encoding a stream of user data bits into a binary d,k channel bitstream (3) comprising a number of sections of respectively N successive RLL channel bits, called RLL rows (8-13, 45), wherein parameter d defines a minimum number and parameter k defines a maximum number of zeroes between any two ones of said bitstream (3) or vice versa,

wherein each RLL row (8-13, 45) represents a parity-check code-word, called row parity-check code-word in which a so-called row-based parity-check constraint for said RLL row (8-13, 45) has been realized,

characterized in that

said encoding means being designed for generating K sections of respectively N successive channel bits, called column parity-check rows (21, 22, 43, 44, 46), at predetermined positions of a group of M RLL rows (8-13, 45), K, N and M being integer values, said column parity-check rows (21, 22, 43, 44, 46) comprising a plurality of column parity-check enabling channel words (30, 42, 48), wherein each of said column parity-check enabling channel words (30, 42, 48) realizes a so-called column-based parity-check constraint for all so-called corresponding segments (24-29) of at least said M RLL rows (8-13, 45) of said group that correspond to a specific column parity-check enabling channel word (30, 42, 48), hereby constituting a column parity-check codeword.

34. (currently amended) A device according to claim 33, characterized in that said device comprising means for performing a

method according to claims 31 ~~or 32~~ in order to generate a signal according to any one of claims 1 to ~~30~~ 28 or 49 to 51.

35. (currently amended) A method for decoding a signal according to ~~any one of claims 1 to 30 or a signal being encoded according to a method of claim 31 or 32~~ claim 1, comprising the steps of:

checking for each RLL row (8-13, 45) a so-called row-based parity-check constraint,

checking for each column parity-check segment (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) that correspond to said column parity-check enabling channel word (30, 42, 48), and

determining an erroneous channel word (51) based on said checking steps.

36. (original) A method according to claim 35, wherein said determining step includes locating an erroneous segment (33, 51) at a crossing point of

a) an erroneous RLL row (31, 52) that violates said row-based parity-check constraint for said RLL row and

b) an erroneous column (32, 53) comprising all corresponding segments (24-29) that correspond to a specific column parity-check enabling channel word (30, 42, 48), wherein said column (32, 53) violates said column-based parity-check constraint.

37. (original) A method according to claim 36, wherein an located erroneous segment (33, 51) is corrected if a single erroneous segment occurs.

38. (original) A method according to claim 35, wherein said determining step is further based on channel side-information if more than a single erroneous segment (33, 51) occurs.

39. (original) A method according to claim 38, wherein said channel side-information is phase-error information of bit transitions in the channel words of the segments at said crossing points.

40. (original) A method according to claim 39, wherein a phase-error with the largest absolute value is determined and the corresponding one-bit of the d,k channel bitstream (3) is shifted by one bit position.

41. (original) A method according to claim 35, wherein said signal comprises said column parity-check enabling channel words (30, 42, 48) at every second channel bit position only, and wherein said determining step includes, upon detecting a first erroneous column (32, 53), the step of deciding whether another erroneous column is positioned to the left or to the right of said first erroneous column (32, 53).

42. (original) A method according to claim 41, wherein said decision step is based on channel-side information.

43. (original) A method according to claim 35, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined internal of such a segment (24-29), namely
a) a transition-shift error is determined from bit position i to the right to bit position $i+1$, if the detected column-based parity-check constraint is detected as

$V_{as\text{-}detected} = N_d(i+1) - N_d(i)$

and

b) a transition-shift error is determined from bit position i to the left to bit position i-1, if the detected column-based parity-check constraint is detected as

$V_{as\text{-}detected} = N_d(i-1) - N_d(i)$

wherein N_d (i-1), N_d (i) N_d (i+1) are the numbers of possible d,k constrained sequences of length i - 1, i, i + 1, respectively.

44. (original) A method according to claim 35, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined crossing the left boundary of such a segment (24-29), namely
a) a transition-shift error is determined from the last bit position of the previous segment (24-29) to the first bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{as\text{-}detected,\,present} = +N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{as\text{-}detected,\,previous} = -N_d(N_{1,2} - 1)$

or

b) a transition-shift error is determined from the first bit position of the present segment (24-29) to the last bit position of the previous segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{as\text{-}detected,\,present} = -N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{as\text{-}detected,\,previous} = +N_d(N_{1,2} - 1)$

wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

45. (original) A method according to claim 35, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined crossing the right boundary of such a segment (24-29), namely
a) a transition-shift error is determined from the last bit position of the present segment (24-29) to the first bit position of the subsequent segment (24-29), if the detected column-based parity-check constraint is detected for the present column as
$V_{as\text{-}detected,\ present} = -N_d(N_{1,2}-1)$
and if the detected column-based parity-check constraint is detected for the subsequent column as
$V_{as\text{-}detected,\ subsequent} = +N_d(0)$
or
b) a transition-shift error is determined from the first bit position of the subsequent segment (24-29) to the last bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as
$V_{as\text{-}detected,\ present} = +N_d(N_{1,2}-1)$
and if the detected column-based parity-check constraint is detected for the subsequent column as
$V_{as\text{-}detected,\ subsequent} = -N_d(0)$
wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

46. (original) A method according to claim 43, wherein a segment (24-29) with a determined single-bit transition-shift error is

corrected by being replaced by a segment (24-29) having said unique index

$w_j = w'_j - V_{\text{as-detected}}$

wherein w'_j is an as-detected index of said segment (24-29) to be replaced, wherein

$$w'_j = \sum_{i=0}^{N_{1,2}-1} b'^j_i \cdot N_d(i)$$

wherein b'^j_i denotes as-detected bit-value for the bit with number i of said segment (24-29) in row j and wherein $N_d(i)$ is the number of possible d,k constrained sequences of length i.

47. (currently amended) A device for decoding a signal according to ~~any one of claims 1 to 30 or a signal being encoded according to a method of claim 31 or 32~~ claim 1, comprising:

- parity-check means for checking for each RLL row (8-13, 45) a row-based parity-check constraint, and for checking for each column parity-check enabling channel word (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said M RLL rows (8-13, 45) that correspond to said column parity-check enabling channel word (30, 42, 48), and
- determining means for determining an erroneous channel word (51) based on the result of said parity-checking.

48. (original) A device according to claim 47, wherein said device comprising means for performing a method according to any one of claims 35 to 46.

49. (new) A signal according to claim 22, characterized in that said parity-check constraint is

$$V = \text{Mod}\left[\sum_{j=1}^{M+1} w_j, q_1\right]$$

being set to a predetermined value at the encoder, known at the decoder, and is preferably set to 0, wherein j is a unique index associated with each RLL row (8-13, 45) for $1 \leq j \leq M$ and an index associated with the actual column parity-check row for $j = M + 1$, and

wherein w_j is a unique index associated with each word W_j which defines one of a number of possible d,k constrained sequences of said segment width (N_1, N_2), wherein such a word W_j is comprised in each corresponding segment.

50. (new) A signal according to claim 26, characterized in that said unique index w_j is

$$w_j = \sum_{i=0}^{N_{1,2}-1} b_i^j \cdot N_d(i)$$

wherein b_i^j denotes bit number i of word W_j in row j and wherein $N_d(i)$ is the number of possible d,k constrained sequences of length i.

51. (new) A signal according to claim 49, characterized in that said unique index w_j is

$$w_j = \sum_{i=0}^{N_{1,2}-1} b_i^j \cdot N_d(i)$$

wherein b_i^j denotes bit number i of word W_j in row j and wherein $N_d(i)$ is the number of possible d,k constrained sequences of length i.

52. (new) A method according to claim 31, characterized by storing the signal on a storage medium.

53. (new) A method according to claim 32, characterized by storing the signal on a storage medium.

54. (new) A device according to claim 33, characterized in that said device comprising means for performing a method according to claim 32.

55. (new) A device according to claim 33, characterized in that said device comprising means for storing the signal on a storage medium.

56. (new) A device according to claim 34, characterized in that said device comprising means for storing the signal on a storage medium.

57. (new) A method for decoding a signal according to any one of claims 35-47, further comprising reading the signal from a storage medium.

58. (new) A method of decoding a signal according to any one of claims 2 to 28 or 49 to 51 or a signal encoded according to the method of claim 31, comprising the steps of:

checking for each RLL row (8-13, 45) a so-called row-based parity-check constraint,

checking for each column parity-check segment (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) that correspond to said column parity-check enabling channel word (30, 42, 48), and

determining an erroneous channel word (51) based on said checking steps.

59. (new) A method according to claim 58, wherein said determining step includes locating an erroneous segment (33, 51) at a crossing point of

a) an erroneous RLL row (31, 52) that violates said row-based parity-check constraint for said RLL row and

b) an erroneous column (32, 53) comprising all corresponding segments (24-29) that correspond to a specific column parity-check enabling channel word (30, 42, 48), wherein said column (32, 53) violates said column-based parity-check constraint.

60. (new) A method according to claim 59, wherein an located erroneous segment (33, 51) is corrected if a single erroneous segment occurs.

61. (new) A method according to claim 58, wherein said determining step is further based on channel side-information if more than a single erroneous segment (33, 51) occurs.

62. (new) A method according to claim 61, wherein said channel side-information is phase-error information of bit transitions in the channel words of the segments at said crossing points.

63. (new) A method according to claim 62, wherein a phase-error with the largest absolute value is determined and the corresponding one-bit of the d,k channel bitstream (3) is shifted by one bit position.

64. (new) A method according to claim 58, wherein said signal comprises said column parity-check enabling channel words (30, 42, 48) at every second channel bit position only, and wherein said determining step includes, upon detecting a first erroneous column (32, 53), the step of deciding whether another erroneous column is

positioned to the left or to the right of said first erroneous column (32, 53).

65. (new) A method according to claim 64, wherein said decision step is based on channel-side information.

66. (new) A method according to claim 58, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined internal of such a segment (24-29), namely
a) a transition-shift error is determined from bit position i to the right to bit position $i+1$, if the detected column-based parity-check constraint is detected as

$$V_{\text{as-detected}} = N_d(i+1) - N_d(i)$$

and
b) a transition-shift error is determined from bit position i to the left to bit position $i-1$, if the detected column-based parity-check constraint is detected as

$$V_{\text{as-detected}} = N_d(i-1) - N_d(i)$$

wherein N_d $(i-1)$, N_d (i) N_d $(i+1)$ are the numbers of possible d,k constrained sequences of length $i-1$, i, $i+1$, respectively.

67. (new) A method according to claim 58, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined crossing the left boundary of such a segment (24-29), namely
a) a transition-shift error is determined from the last bit position of the previous segment (24-29) to the first bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = +N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{\text{as-detected, previous}} = -N_d(N_{1,2}-1)$

or

b) a transition-shift error is determined from the first bit position of the present segment (24-29) to the last bit position of the previous segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = -N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{\text{as-detected, previous}} = +N_d(N_{1,2}-1)$

wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

68. (new) A method according to claim 58, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and wherein a single-bit transition-shift error is determined crossing the right boundary of such a segment (24-29), namely

a) a transition-shift error is determined from the last bit position of the present segment (24-29) to the first bit position of the subsequent segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = -N_d(N_{1,2}-1)$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$V_{\text{as-detected, subsequent}} = +N_d(0)$

or

b) a transition-shift error is determined from the first bit position of the subsequent segment (24-29) to the last bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = +N_d(N_{1,2}-1)$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$V_{\text{as-detected, subsequent}} = -N_d(0)$

wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

69. (new) A method according to claim 66, wherein a segment (24-29) with a determined single-bit transition-shift error is corrected by being replaced by a segment (24-29) having said unique index

$w_j = w'_j - V_{\text{as-detected}}$

wherein w'_j is an as-detected index of said segment (24-29) to be replaced, wherein

$$w'_j = \sum_{i=0}^{N_{1,2}-1} b'^j_i \cdot N_d(i)$$

wherein b'^j_i denotes as-detected bit-value for the bit with number i of said segment (24-29) in row j and wherein N_d (i) is the number of possible d,k constrained sequences of length i.

70. (new) A method of decoding a signal encoded according to the method of claim 32, comprising the steps of:

checking for each RLL row (8-13, 45) a so-called row-based parity-check constraint,

checking for each column parity-check segment (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said M RLL rows (8-13, 45) that

correspond to said column parity-check enabling channel word (30, 42, 48), and

determining an erroneous channel word (51) based on said checking steps.

71. (new) A method according to claim 70, wherein said determining step includes locating an erroneous segment (33, 51) at a crossing point of

a) an erroneous RLL row (31, 52) that violates said row-based parity-check constraint for said RLL row and

b) an erroneous column (32, 53) comprising all corresponding segments (24-29) that correspond to a specific column parity-check enabling channel word (30, 42, 48), wherein said column (32, 53) violates said column-based parity-check constraint.

72. (new) A method according to claim 71, wherein an located erroneous segment (33, 51) is corrected if a single erroneous segment occurs.

73. (new) A method according to claim 70, wherein said determining step is further based on channel side-information if more than a single erroneous segment (33, 51) occurs.

74. (new) A method according to claim 73, wherein said channel side-information is phase-error information of bit transitions in the channel words of the segments at said crossing points.

75. (new) A method according to claim 74, wherein a phase-error with the largest absolute value is determined and the corresponding one-bit of the d,k channel bitstream (3) is shifted by one bit position.

76. (new) A method according to claim 70, wherein said signal comprises said column parity-check enabling channel words (30, 42, 48) at every second channel bit position only, and wherein said determining step includes, upon detecting a first erroneous column (32, 53), the step of deciding whether another erroneous column is positioned to the left or to the right of said first erroneous column (32, 53).

77. (new) A method according to claim 76, wherein said decision step is based on channel-side information.

78. (new) A method according to claim 70, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and
wherein a single-bit transition-shift error is determined internal of such a segment (24-29), namely
a) a transition-shift error is determined from bit position i to the right to bit position $i+1$, if the detected column-based parity-check constraint is detected as
$V_{as\text{-}detected} = N_d(i+1) - N_d(i)$
and
b) a transition-shift error is determined from bit position i to the left to bit position $i-1$, if the detected column-based parity-check constraint is detected as
$V_{as\text{-}detected} = N_d(i-1) - N_d(i)$

wherein N_d $(i-1)$, N_d (i) N_d $(i+1)$ are the numbers of possible d,k constrained sequences of length $i - 1$, i, $i + 1$, respectively.

79. (new) A method according to claim 70, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and

wherein a single-bit transition-shift error is determined crossing the left boundary of such a segment (24-29), namely

a) a transition-shift error is determined from the last bit position of the previous segment (24-29) to the first bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = +N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{\text{as-detected, previous}} = -N_d(N_{1,2} - 1)$

or

b) a transition-shift error is determined from the first bit position of the present segment (24-29) to the last bit position of the previous segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = -N_d(0)$

and if the detected column-based parity-check constraint is detected for the previous column as

$V_{\text{as-detected, previous}} = +N_d(N_{1,2} - 1)$

wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

80. (new) A method according to claim 70, wherein said signal comprises segments (24-29) of more than one successive channel bits of alternating segment width N_1 or N_2, and

wherein a single-bit transition-shift error is determined crossing the right boundary of such a segment (24-29), namely

a) a transition-shift error is determined from the last bit position of the present segment (24-29) to the first bit position of the subsequent segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = -N_d(N_{1,2} - 1)$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$V_{\text{as-detected, subsequent}} = +N_d(0)$

or

b) a transition-shift error is determined from the first bit position of the subsequent segment (24-29) to the last bit position of the present segment (24-29), if the detected column-based parity-check constraint is detected for the present column as

$V_{\text{as-detected, present}} = +N_d(N_{1,2} - 1)$

and if the detected column-based parity-check constraint is detected for the subsequent column as

$V_{\text{as-detected, subsequent}} = -N_d(0)$

wherein N_d (0) = 1 and N_d ($N_{1,2}$ - 1) is the number of possible d,k constrained sequences of length $N_{1,2}$ - 1.

81. (new) A method according to claim 78, wherein a segment (24-29) with a determined single-bit transition-shift error is corrected by being replaced by a segment (24-29) having said unique index

$w_j = w'_j - V_{\text{as-detected}}$

wherein w'_j is an as-detected index of said segment (24-29) to be replaced, wherein

$$w'_j = \sum_{i=0}^{N_{1,2}-1} b'^j_i \cdot N_d(i)$$

wherein b'^j_i denotes as-detected bit-value for the bit with number i of said segment (24-29) in row j and wherein N_d (i) is the number of possible d,k constrained sequences of length i.

82. (new) A device for decoding a signal according to any one of claims 2 to 28 or 49 to 51 or a signal encoded according to the method of claim 31, comprising:

- parity-check means for checking for each RLL row (8-13, 45) a row-based parity-check constraint, and for checking for each column parity-check enabling channel word (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) that correspond to said column parity-check enabling channel word (30, 42, 48), and
- determining means for determining an erroneous channel word (51) based on the result of said parity-checking.

83. (new) A device for decoding a signal encoded according to the method of claim 32, comprising:

- parity-check means for checking for each RLL row (8-13, 45) a row-based parity-check constraint, and for checking for each column parity-check enabling channel word (30, 42, 48) of said column parity-check rows (21, 22, 43, 44, 46) a so-called column-based parity-check constraint along all corresponding segments (24-29) of at least said *M* RLL rows (8-13, 45) that correspond to said column parity-check enabling channel word (30, 42, 48), and
- determining means for determining an erroneous channel word (51) based on the result of said parity-checking.